Room Temperature Topological Insulator Spintronics: Demonstration of Perpendicular Magnetization Switching and Unidirectional Spin Hall Magnetoresistance

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Room temperature non-volatile spintronic devices possess unique advantages as key building blocks for future computing, memory and analog electronic systems. Recent developments show that topological insulators hold significant promise as an alternative materials platform for such spintronic devices. Hybrid structures that interface topological surface states with magnetism show promising spintronic device related phenomena such as extremely efficient charge-to-spin conversion at room temperature. I will first review the roadblocks remaining for developing topological spintronics into a viable technology.

I will report our recent effort to design and implement write and read functions of spintronic devices based on topological insulators and their hybrid structures: 1) a demonstration of unidirectional spin Hall magnetoresistance in TI/CoFeB heterostructures for direct read function implementation [1]; 2) a recent demonstration of perpendicular magnetization switching through giant spin-orbit torque from sputtered $Bi_xSe_{(1-x)}$ film [2]; We investigated the spin-orbit torque (SOT) in $Bi_xSe_{(1-x)}$/CoFeB heterostructures by using dc planar Hall and spin-torque ferromagnetic resonance (ST-FMR) methods. Remarkably, the spin Hall angle (SHA) was determined to be as large as 18.62 ± 0.13 and 8.67 ± 1.08, using the dc planar Hall and ST-FMR methods, respectively. Moreover, switching of perpendicular CoFeB multilayers using SOT from the $Bi_xSe_{(1-x)}$ has been observed at room temperature (RT) with the lowest-ever switching current density reported in a bilayer system 4.3×10^5 A/cm^2. The demonstrated giant SHA, ease of growth of the films on a silicon substrate, and successful growth and switching of a perpendicular CoFeB multilayer on $Bi_xSe_{(1-x)}$ film provide an avenue for the use of the topological insulator (TI) $Bi_xSe_{(1-x)}$ as a spin-current generator in SOT-based memory and logic devices.

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Reference

[1] Y. Lv et al., submitted and under revision (2017); **arXiv:1701.06505**
[2] Mahendra DC et al., submitted (2017); **arXiv:1703.03822**